### Harold's Boolean Algebra Cheat Sheet

8 September 2025

# **Boolean Algebra**

Boolean Law	Boolean Expression	Equivalent Circuit	Description
Idempotent	A + A = A	A	A in parallel with A = "A"
idempotent	$A \bullet A = A$	A A	A in series with A = "A"
Associative	$A + (B + C)$ $= (A + B) + C$ $= A + B + C$ $A \cdot (B \cdot C)$ $= (A \cdot B) \cdot C$ $= A \cdot B \cdot C$		Allows the removal of brackets from an expression and the regrouping of the variables
Communitativa	A + B = B + A	A	A in parallel with B = B in parallel with A
Commutative	$A \bullet B = B \bullet A$		A in series with B = B in series with A
Distributive	$A \bullet (B + C)$ $= A \bullet B + A \bullet C$ $A + B \bullet C =$ $(A + B) \bullet (A + C)$		Permits the multiplying or factoring out of an expression
	$(A+B) \bullet (A+C)$ $A+0=A$	A	A in parallel with open = "A"
Identity	$A \bullet 1 = A$	A	A in series with closed = "A"
Domination	A + 1 = 1	A	A in parallel with closed = "CLOSED"
(Annulment)	$A \bullet 0 = 0$		A in series with open = "OPEN"
Double Compliment (Double Negation)	$\overline{\overline{A}} = A$		NOT NOT A (double negative) = "A"

Complement	$A + \overline{A} = 1$	Ā	A in parallel with NOT A = "CLOSED"
Complement	$A\bullet \overline{A}=0$	A Ā	A in series with NOT A = "OPEN"
De Mergen's	$\overline{(A+B)} = \overline{A} \bullet \overline{B}$		Invert and replace OR with AND
De Morgan's	$\overline{A \bullet B} = \overline{A} + \overline{B}$		Invert and replace AND with OR
	A + (AB) = A		Enables a reduction in a
Absorption	A(A+B)=A		complicated expression to a simpler one by absorbing like terms
(Absorptive)	$A + \overline{A}B = A + B$		Reduces a complicated expression to a simpler one by absorbing complement term

### **Precedence Rules**

#	Operator	Symbol	Precedence
1	Parenthesis	( )	Highest precedence
2	NOT	~	
3	Quantifiers	∀,∃	
4	AND	•	Applied Left to Right
5	OR	V	
6	Conditional	n	
7	Biconditional	$\leftrightarrow$	Lowest precedence

## **Boolean Logic Gates**

Boolean Logic	Notation	Gate	Description
IDENTITY	1 T True S	VCC 5V V+ ↑ ↑ ↑	On, Tautology, High voltage (typically +5V)
NULL	0 F False ⊥ Ø	GND = ///	Off, Contradiction, Low voltage (typically 0V)
Input	A, B, C, D		Line, Wire, Connects to
Output	W, X, Y, Z		Line, Wire, Connects from
AND	A • B AB A. B A ∧ B A ∩ B	AQ	AND, BUT, Multiply, Conjunction, Intersection
OR	A + B A V B A U B A   B	AQ	Inclusive-OR, Add, Disjunction, Union
NOT	Ā A^ A' ¬A ~A ! A	A — Q	NOT, Invert, Negation, Change, Difference
NAND	A • B AB A ⊼ B A   B*	AQ	Not AND
NOR	$ \overline{A + B}  A \overline{\vee} B  A \downarrow B $	A B	Not OR
XOR	$A \bigoplus B$ $A \veebar B$ $A\overline{B} + \overline{A}B$	A B	Exclusive-OR, Both A and B are different
XNOR	$ \begin{array}{c} A \odot B \\ \overline{A \oplus B} \\ AB + \overline{AB} \end{array} $	AQ	Exclusive-NOR, Both A and B are the same

**NOTE:** The laws of Boolean algebra are the same in propositional and set logic.

# **Boolean Logic Truth Tables**

Inp	uts	Outputs								
Α	В	AND .	NAND ⊼	OR +	NOR ⊽	XOR ⊕	XNOR  ⊙	$\frac{\mathbf{NOT}}{\overline{A}}$	VCC 1	GND 0
0	0	0	1	0	1	0	1	A=1	1	0
0	1	0	1	1	0	1	0	A=1	1	0
1	0	0	1	1	0	1	0	A=0	1	0
1	1	1	0	1	0	0	1	A=0	1	0

### **Blank Truth Tables**

Inp	uts	Output
Α	В	Х
0	0	
0	1	
1	0	
1	1	

	Input	Out	put	
Α	В	С	Х	Υ
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

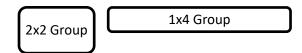
	Inputs				Dutpu	t
Α	В	С	D	Х	Υ	Z
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

#### **Karnaugh Mapping (K-Map)**

2-Bit			A
K-N	K-Map		1
D	0		
В	1		

3-	Bit	AB			
K-N	K-Map		01	11	10
_	0				
<b>C</b> 1					

4-	Bit	AB			
K-N	Лар	00	01	11	10
	00				
CD	01				
CD	11				
	10				



#### **K-Map Rules**

- 1) Circle only 1s (ones) and don't cares for Sum of Products (SOP),  $e.g.~\overline{A}~\overline{B}~\overline{C} + \overline{A}BC + AB\overline{C}$ .
  - a. Circle only 0s (zeros) and don't cares for Product of Sums (POS), e. g.  $(A + \overline{B})(\overline{A} + B)$ .
  - b. Don't cares may be used or ignored.
- 2) No diagonals, only horizontal or vertical connections.
- 3) Group only adjacent cells in groups with powers of 2 (1x1, 1x2, 2x1, 2x2, 2x4, 4x2, 1x4, 4x1).
- 4) Make groups as large as possible.
- 5) Must group all 1s (ones) for SOP or all 0s (zeros) for POS.
- 6) Overlapping is allowed.
- 7) Wrapping around all edges allowed, both top-bottom edges and left-right edges.
- 8) Fewest groups possible (OPTIMAL).
- 9) For each circle, determine which inputs do not contribute to the logic (is both 0 and 1).
- 10) Write down the equation as a SOP,  $e. g. \overline{A} \overline{B} \overline{C} + \overline{A}BC + AB\overline{C}$

#### Sources

- <u>SNHU MAT 230</u> Discrete Mathematics, zyBooks.
- https://www.electronics-tutorials.ws/boolean/bool 6.html
- Toomey, H. A. (2024). Logical Connective Laws, <u>Harold's Logic Cheat Sheet</u>, https://www.toomey.org/tutor/discrete\_math.html

#### See Also

- Harold's Logic Cheat Sheet
- Harold's Logic (Philosophy) Cheat Sheet
- Harold's Sets Cheat Sheet
- Harold's Boolean Algebra Cheat Sheet
- Harold's Proofs Cheat Sheet